Dual N-Channel 30 V (D-S) MOSFET with Schottky Diode

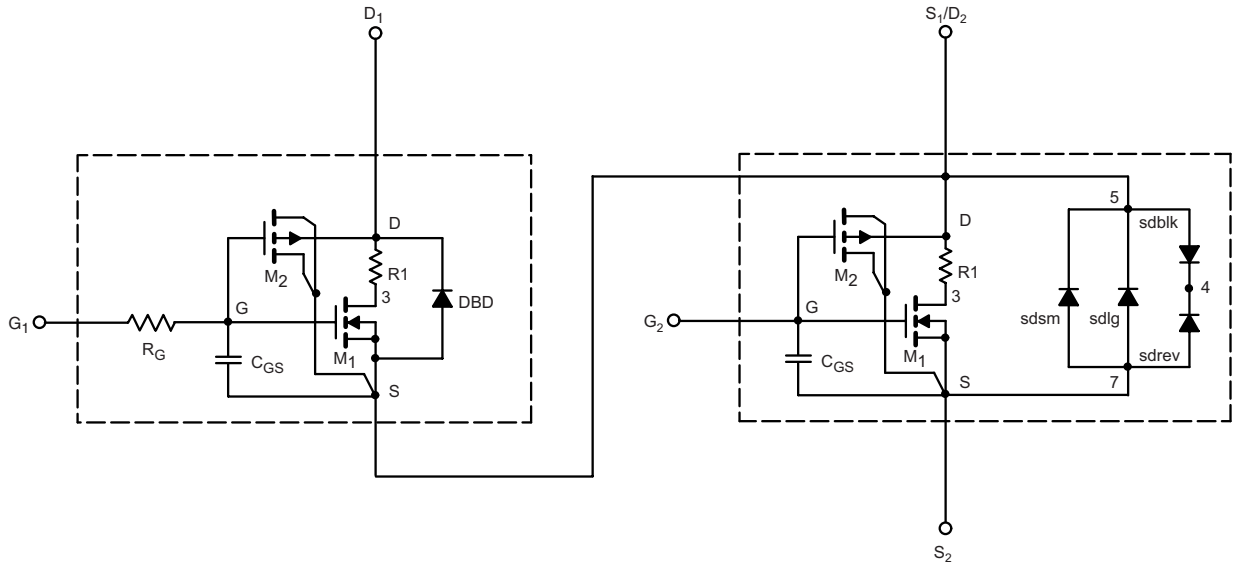
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

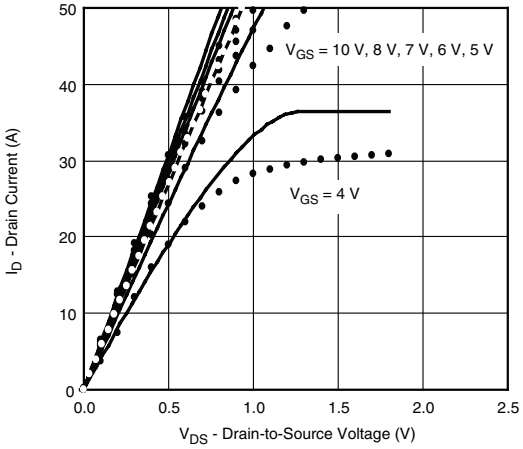
SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	Ch-1	2	-	V
			Ch-2	2	-	
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 8 A	Ch-1	0.0162	0.0165	Ω
		V_{GS} = 10 V, I_D = 8 A	Ch-2	0.0153	0.0155	
		V_{GS} = 4.5 V, I_D = 6 A	Ch-1	0.0217	0.0215	
		V_{GS} = 4.5 V, I_D = 6 A	Ch-2	0.022	0.020	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 8 A	Ch-1	25	29	S
		V_{DS} = 15 V, I_D = 8 A	Ch-2	24	33	
Diode Forward Voltage[b]	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V	Ch-1	0.78	0.77	V
		I_S = 1 A, V_{GS} = 0 V	Ch-2	0.45	0.46	
Dynamic[b]						
Total Gate Charge	Q_g	Channel 1 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 8 A Channel 2 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 8 A	Ch-1	6.8	6.7	nC
			Ch-2	7	7	
Gate-Source Charge	Q_{gs}		Ch-1	2.8	2.2	
			Ch-2	2.8	2.8	
Gate-Drain Charge	Q_{gd}		Ch-1	2	2	
			Ch-2	2	2	

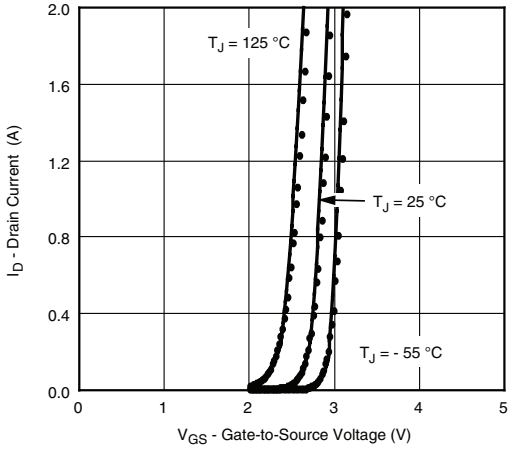
Notes

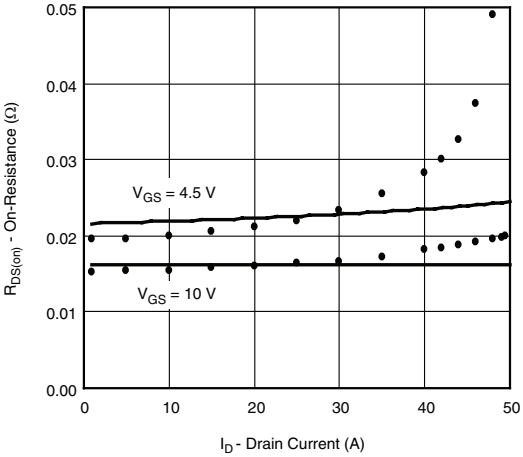
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

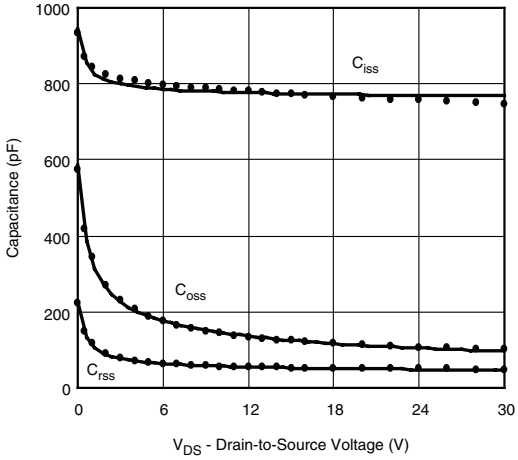
b. Guaranteed by design, not subject to production testing.

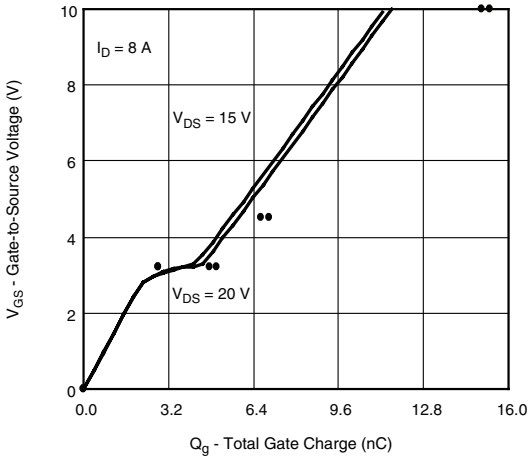
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted
Channel 1

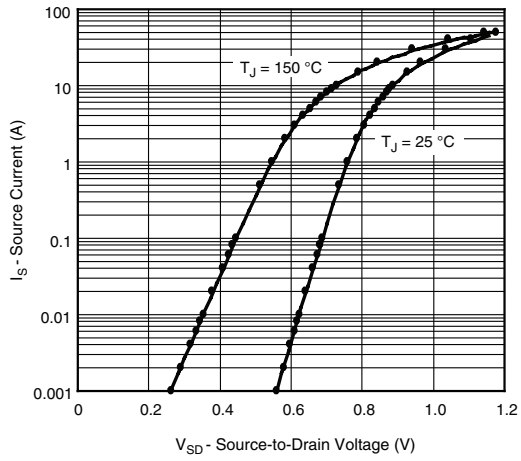








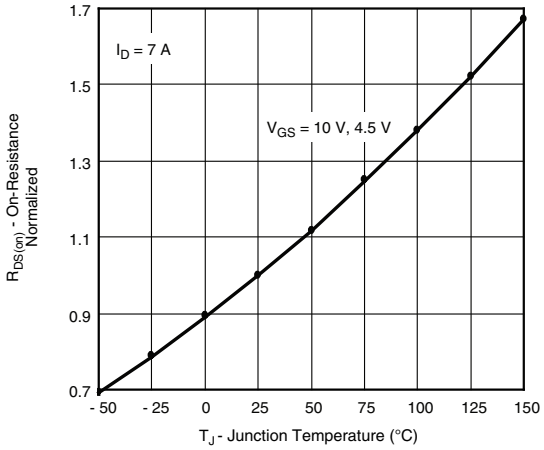


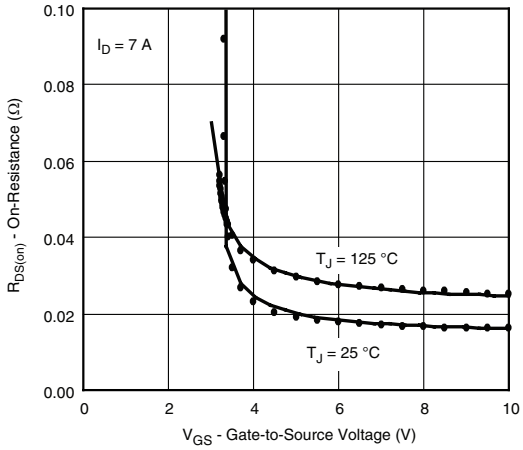


Note
Dots and squares represent measured data.

COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

Channel 1





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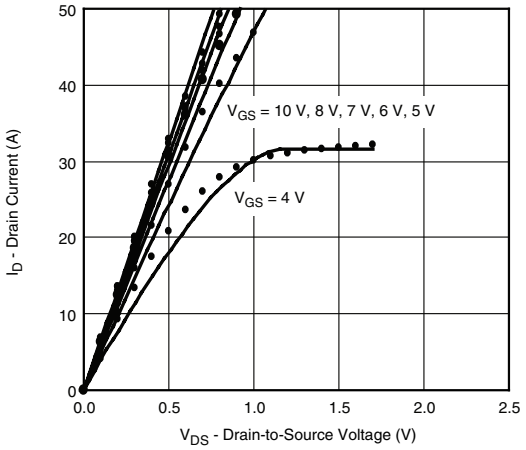
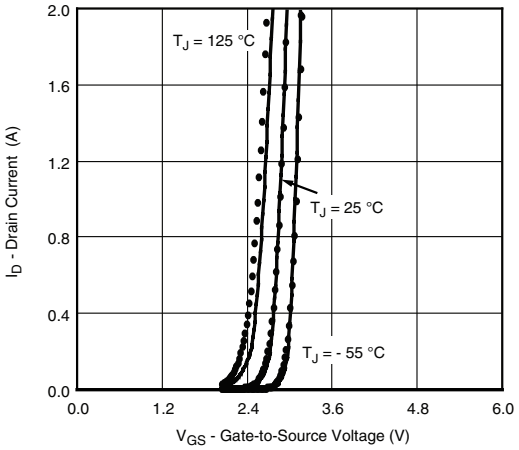
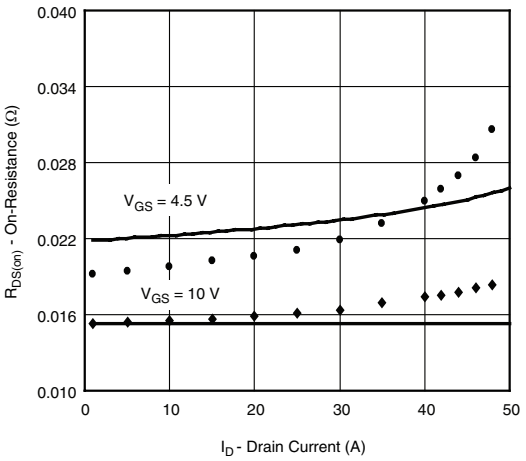
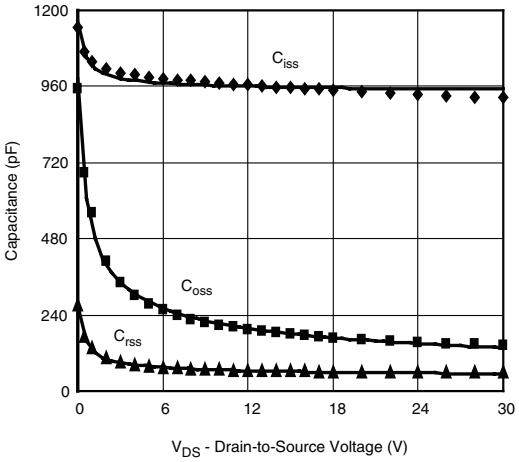
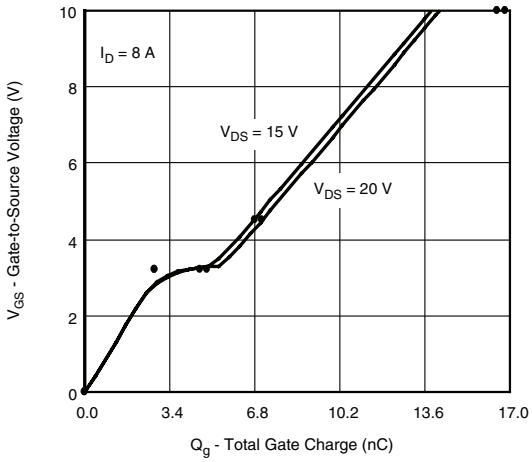
Channel 2

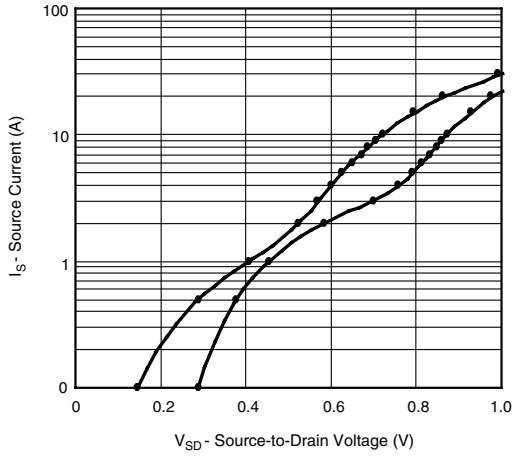












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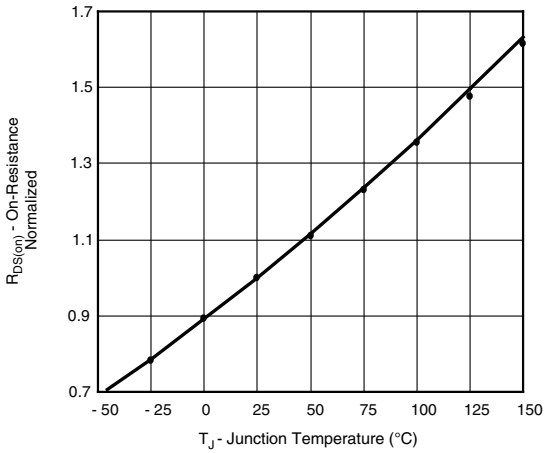

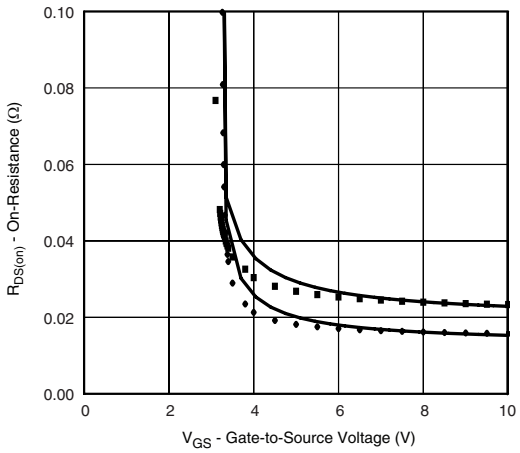

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